

Appl. No. 10/810,759  
Reply to Examiner's Action dated November 23, 2005

**REMARKS/ARGUMENTS**

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-18 in the application. Presently, the Applicants have added new Claims 19-20. No other claims have been amended, cancelled or added. Accordingly, Claims 1-20 are currently pending in the application.

**I. Rejection of Claims 1-3, 7 and 9 under 35 U.S.C. §102**

The Examiner has rejected Claims 1-3, 7 and 9 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,821,887 to Kim ("Kim"). Independent Claims 1 and 10 currently include the element of forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate electrode in a different step. Kim fails to disclose this element.

Kim is directed to a method of making a MOS transistor. (Title). Kim teaches that a gate structure comprising a gate oxide 24, a polysilicon gate electrode 25, a self-aligned silicided layer 27 formed from the polysilicon gate electrode 25, and spacers 26, is formed over a semiconductor substrate 21 having source/drain regions 23 and self-aligned silicided layers 27. Kim then teaches that this structure undergoes a number of processing steps before an insulating layer 29 is formed over and protecting the source/drain regions 23 and self-aligned silicided layers 27. Kim then teaches that a metal layer 30 is formed over the exposed self-aligned silicided layer 27 that was

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previously formed from the polysilicon gate electrode 25, but that the insulating layer 20 protects the source/drain regions 23 and self-aligned silicided layers 27 from the metal layer 30. Thereafter, the metal layer 30 is subjected to a thermal treatment process to transform completely the polysilicon gate electrode 25 into a metal silicided gate electrode 31, the metal layer 30 having no effect on the source/drain regions 23 and self-aligned silicided layers 27 because of the insulating layer 29.

The Examiner asserts that the self-aligned silicided layers 27 located within the source/drain regions 23 are acting as a blocking layer, as is presently claimed. The Applicants respectfully disagree with the Examiner on this point. Namely, the self-aligned silicided layers 27 are not acting as blocking layers, as Kim requires that the insulating layer 29 be formed thereover to act as the blocking layer. Accordingly, were the self-aligned silicided layers 27 to actually act as blocking layers, there would have been no need for the insulating layer 29. Therefore, Kim fails to disclose forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate electrode in a different step, as is presently claimed.

Therefore, Kim does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 2-3, 7 and 9 are dependent upon Claim 1, Kim also cannot be an anticipating reference for Claims 2-3, 7 and 9. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to these Claims.

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## II. Rejection of Claims 4-6 and 8 under 35 U.S.C. §103

The Examiner has rejected Claims 4-6 and 8 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of U.S. Patent No. 6,821,887 to Wieczorek, *et al.* ("Wieczorek"). As previously indicated, independent Claims 1 and 10 currently include the element of forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate electrode in a different step. As previously established, Kim fails to disclose these elements. Kim further fails to suggest these elements. Namely, Kim fails to suggest these elements because Kim specifically requires forming an insulator layer 29 over the self-aligned silicided layers 27 located within the source/drain regions 23 to act as a blocking layer, as well as for the protection of the self-aligned silicided layers 27 located within the source/drain regions 23. Were the self-aligned silicided layers 27 to actually act as blocking layers, no insulator layer 29 would be required. Accordingly, Kim further fails to suggest these elements.

Wieczorek fails to correct the deficiencies of Kim. The Examiner is offering Wieczorek for the sole proposition that the silicided gate electrode and metal silicided regions may comprise different materials, and that the blocking layer may have a thickness ranging from about 10 nm to about 35 nm. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion that the silicided gate electrode and metal silicided regions may comprise different materials, and that the blocking layer may have a thickness ranging from about 10 nm to about 35 nm is entirely different from a teaching or suggestion of forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate

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electrode in a different step, as is currently claimed. Accordingly, Wieczorek also fails to teach or suggest this claimed element.

Therefore, Kim alone or in combination with Wieczorek, fails to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole. Accordingly, the combination fails to establish a *prima facie* case of obviousness with respect to these claims. Claims 4-6 and 8 are therefore not obvious in view of the combination.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 4-6 and 8 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

### III. Rejection of Claims 10-12, 16 and 18 under 35 U.S.C. §103

The Examiner has rejected Claims 10-12, 16 and 18 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of U.S. Patent No. 6,830,987 to Pelella, *et al.* ("Pelella"). As previously indicated, independent Claims 1 and 10 currently include the element of forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate electrode in a different step. As established above, Kim fails to teach or suggest this element.

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Pelella fails to correct the deficiencies of Kim. The Examiner is offering Pelella for the sole proposition of forming interconnects within dielectrics located over the substrate. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion of forming interconnects within dielectrics located over the substrate is entirely different from a teaching or suggestion of forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate electrode in a different step, as is currently claimed. Accordingly, Pelella also fails to teach or suggest this claimed element.

Therefore, Kim alone or in combination with Pelella, fails to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole. Accordingly, the combination fails to establish a *prima facie* case of obviousness with respect to these claims. Claims 10-12, 16 and 18 are therefore not obvious in view of the combination.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 10-12, 16 and 18 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

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**IV. Rejection of Claims 13-15 and 17 under 35 U.S.C. §103**

The Examiner has rejected Claims 13-15 and 17 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Pelella and further in view of Wieczorek. As previously indicated, independent Claims 1 and 10 currently include the element of forming a blocking layer over source/drain regions in a step, the blocking layer comprising a metal silicided, and forming a silicided gate electrode in a different step. As established above, each of Kim, Pelella and Wieczorek individually fail to teach or suggest this element. Accordingly, the combination must also fail to teach or suggest this element.

Therefore, Kim alone or in combination with Pelella and/or Wieczorek, fails to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole. Accordingly, the combination fails to establish a *prima facie* case of obviousness with respect to these claims. Claims 13-15 and 17 are therefore not obvious in view of the combination.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 13-15 and 17 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

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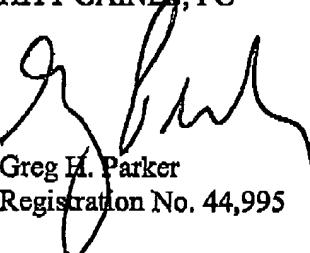
**V. Conclusion**

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 20-0668.

Respectfully submitted,

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